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## CMP PROCESS CONTROL METHOD

### Field of the Invention

[001] The present invention relates to chemical mechanical polishing apparatus for polishing semiconductor wafer substrates. More particularly, the present invention relates to an improved CMP process control method which includes a one-time polishing time feedback adjustment for all wafers in a lot to facilitate greater between-wafer uniformity in the quantity of material removed from the wafers in a CMP process.

### Background of the Invention

[002] In the fabrication of semiconductor devices from a silicon wafer, a variety of semiconductor processing equipment and tools are utilized. One of these processing tools is used for polishing thin, flat semiconductor wafers to obtain a planarized surface. A planarized surface is highly desirable on a shadow trench isolation (STI) layer, inter-layer dielectric (ILD) or on an inter-metal dielectric (IMD) layer, which are frequently used in both memory and logic devices. The planarization process is important since it enables the subsequent use of a high-resolution lithographic process to fabricate the next-level circuit. The accuracy of a high resolution lithographic process can be achieved only when the process is carried out on a

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substantially flat surface. The planarization process is therefore an important processing step in the fabrication of semiconductor devices.

[003] A global planarization process can be carried out by a technique known as chemical mechanical polishing, or CMP. The process has been widely used on STI, ILD or IMD layers in fabricating modern semiconductor devices. A CMP process is performed by using a rotating platen in combination with a polishing head. The process is used primarily for polishing the front surface or the device surface of a semiconductor wafer for achieving planarization and for preparation of the next level processing. A wafer is frequently planarized one or more times during a fabrication process in order for the top surface of the wafer to be as flat as possible. A wafer can be polished in a CMP apparatus by being placed on a carrier and pressed face down on a polishing pad covered with a slurry of fumed, colloidal silica, aluminum, or CeO<sub>2</sub>.

[004] A polishing pad used on a rotating platen is typically constructed in two layers overlying a platen, with a resilient layer as an outer layer of the pad. The layers are typically made of a polymeric material such as polyurethane and may include a filler for controlling the dimensional stability of the layers.

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A polishing pad is typically made several times the diameter of a wafer in a conventional rotary CMP, while the wafer is kept off-center on the pad in order to prevent polishing of a non-planar surface onto the wafer. The wafer itself is also rotated during the polishing process to prevent polishing of a tapered profile onto the wafer surface. The axis of rotation of the wafer and the axis of rotation of the pad are deliberately not collinear; however, the two axes must be parallel. It is known that uniformity in wafer polishing by a CMP process is a function of pressure, velocity and concentration of the slurry used.

[005] A CMP process is frequently used in the planarization of an STI, ILD or IMD layer on a semiconductor device. Such layers are typically formed of a dielectric material. A most popular dielectric material for such usage is silicon oxide. In a process for polishing a dielectric layer, the goal is to remove topography and yet maintain good uniformity across the entire wafer. The amount of the dielectric material removed is normally between about 2000 Å and about 10,000 Å. The uniformity requirement for STI, ILD or IMD polishing is very stringent since non-uniform dielectric films lead to poor lithography and resulting window-etching or plug-formation difficulties. The CMP process has also been applied to polishing metals, for instance, in tungsten plug formation and in embedded structures. A metal

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polishing process involves a polishing chemistry that is significantly different than that required for oxide polishing.

[006] Important components used in CMP processes include an automated rotating polishing platen and a wafer holder, which both exert a pressure on the wafer and rotate the wafer independently of the platen. The polishing or removal of surface layers is accomplished by a polishing slurry consisting mainly of fumed, colloidal silica or  $\text{CeO}_2$  suspended in deionized water or alkali solution. The slurry is frequently fed by an automatic slurry feeding system in order to ensure uniform wetting of the polishing pad and proper delivery and recovery of the slurry. For a high-volume wafer fabrication process, automated wafer loading/unloading and a cassette handler are also included in a CMP apparatus.

[007] As the name implies, a CMP process executes a microscopic action of polishing by both chemical and mechanical means. While the exact mechanism for material removal of an oxide layer is not known, it is hypothesized that the surface layer of silicon oxide is removed by a series of chemical reactions which involve the formation of hydrogen bonds with the oxide surface of both the wafer and the slurry particles in a hydrogenation reaction; the formation of hydrogen bonds between the wafer and the slurry; the

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formation of molecular bonds between the wafer and the slurry; and finally, the breaking of the oxide bond with the wafer or the slurry surface when the slurry particle moves away from the wafer surface. It is generally recognized that the CMP polishing process is not a mechanical abrasion process of slurry against a wafer surface.

[008] While the CMP process provides a number of advantages over the traditional mechanical abrasion type polishing process, a serious drawback for the CMP process is the difficulty in controlling polishing rates at different locations on a wafer surface. Since the polishing rate applied to a wafer surface is generally proportional to the relative rotational velocity of the polishing pad, the polishing rate at a specific point on the wafer surface depends on the distance from the axis of rotation. In other words, the polishing rate obtained at the edge portion of the wafer that is closest to the rotational axis of the polishing pad is less than the polishing rate obtained at the opposite edge of the wafer. Even though this is compensated for by rotating the wafer surface during the polishing process such that a uniform average polishing rate can be obtained, the wafer surface, in general, is exposed to a variable polishing rate during the CMP process.

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[009] Recently, a chemical mechanical polishing method has been developed in which the polishing pad is not moved in a rotational manner but instead, in a linear manner. It is therefore named as a linear chemical mechanical polishing process, in which a polishing pad is moved in a linear manner in relation to a rotating wafer surface. The linear polishing method affords a more uniform polishing rate across a wafer surface throughout a planarization process for the removal of a film layer from the surface of a wafer. One added advantage of the linear CMP system is the simpler construction of the apparatus, and this not only reduces the cost of the apparatus but also reduces the floor space required in a clean room environment.

[0010] A typical conventional CMP apparatus 90 is shown in FIG. 1 and includes a base 100; polishing pads 210a, 210b, and 210c provided on the base 100; a head clean load/unload (HCLU) station 360 which includes a load cup 300 for the loading and unloading of wafers (not shown) onto and from, respectively, the polishing pads; and a head rotation unit 400 having multiple polishing pads 410a, 410b, 410c and 410d for holding and fixedly rotating the wafers on the polishing pads.

[0011] The three polishing pads 210a, 210b and 210c facilitate simultaneous processing of multiple wafers in a short time. Each

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of the polishing pads is mounted on a rotatable carousel (not shown). Pad conditioners 211a, 211b and 211c are typically provided on the base 100 and can be swept over the respective polishing pads for conditioning of the polishing pads. Slurry supply arms 212a, 212b and 212c are further provided on the base 100 for supplying slurry to the surfaces of the respective polishing pads.

[0012] The polishing heads 410a, 410b, 410c and 410d of the head rotation unit 400 are mounted on respective rotation shafts 420a, 420b, 420c, and 420d which are rotated by a driving mechanism (not shown) inside the frame 401 of the head rotation unit 400. The polishing heads hold respective wafers (not shown) and press the wafers against the top surfaces of the respective polishing pads 210a, 210b and 210c. In this manner, material layers are removed from the respective wafers. The head rotation unit 400 is supported on the base 100 by a rotary bearing 402 during the CMP process.

[0013] The load cup 300 is detailed in FIG. 1 and includes a pedestal support column 312 that supports a circular pedestal 310 on which the wafers are placed for loading of the wafers onto the polishing pads 210a, 210b and 210c, and unloading of the wafers from the polishing pads. A pedestal film 313 is typically

provided on the upper surface of the pedestal 310 for contacting the patterned surface (the surface on which IC devices are fabricated) of each wafer. Fluid openings 314 extend through the pedestal 310 and pedestal film 313. The bottom surfaces of the polishing heads 410a, 410b, 410c and 410d and the top surface of the pedestal film 313 are washed at the load cup 300 by the ejection of washing fluid through the fluid openings 314.

[0014] In typical operation, the CMP apparatus 90 is used to remove material from a layer (not shown) on each wafer in order to reduce the thickness of the layer to a desired target thickness. Accordingly, the pre-CMP thickness of the layer is initially measured, and the estimated polish time and polish recipe, along with the target thickness for the layer on each wafer, are programmed into a CLC (closed-loop controller) 1, shown in Figure 2. Each wafer is mounted on a polishing head 410a, 410b, 410c or 410d and sequentially polished against the polishing pads 210a, 210b and 210c, respectively, of the CMP apparatus 90. The polishing pads progressively remove material from and reduce the thickness of the layer on the wafer. The polishing process is shown in Figure 2, wherein S1 indicates the first polishing step on the polishing pad 210a; S2 indicates the second polishing step on the polishing pad 210b; and S3 indicates the third polishing step on the polishing pad 210c. The CLC 1



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controls the polish time and other aspects of the polishing recipe at each polishing step in the sequence. After the polishing sequence is completed the wafer may be subjected to post-CMP cleaning, as indicated in step S4.

[0015] After post-CMP cleaning, the wafer may be subjected to in-line metrology, as indicated in step S5, to measure the post-CMP thickness of the polished layer. The post-CMP thicknesses of the layers among the wafers in a given wafer lot have a tendency to vary somewhat from each other, due to the inherent differences in the material removal rate from one polishing sequence to another. Accordingly, the measured post-CMP thickness of the layer on each wafer is transmitted as a feedback signal 2 to the CLC 1, which uses the pre-CMP thickness, post-CMP thickness and polish time for each wafer to calculate the material removal rate for the layer on the wafer. The CLC 1 then uses the calculated material removal rate for the wafer to adjust the polishing time for the next wafer to be polished at the polishing steps S1-S3. Accordingly, a feedback adjustment to the polish time is made to the process recipe for each successive wafer in a wafer lot, and is based on the material removal rate calculated for the layer on the previous wafer. This continuous feedback for each wafer in the lot contributes to uniformity in the quantity of material removed from the layers among the multiple wafers in the lot.

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[0016] The continuous feedback mechanism described above is based on a single-variable (material removal rate) algorithm and is suitable for CMP applications in which material is removed from a single layer on a wafer. However, the continuous feedback mechanism is unsuitable for more complex processes, such as STI (shallow trench isolation) CMP processes. In an STI CMP process, three variables must be taken into account when calculating the proper material removal rate: the trench depth, the HDP oxide thickness and the SiN thickness. Use of the single-variable continuous feedback mechanism in an STI CMP process frequently causes over-prediction and over-adjustment to the material removal rate for succeeding wafers in a lot. Accordingly, an improved method for controlling a CMP process is needed.

[0017] An object of the present invention is to provide an improved CMP process control method.

[0018] Another object of the present invention is to provide an improved, one-time feedback CMP process control method which contributes to uniformity in the quantity of material removed from wafers in a lot during semiconductor processing.

[0019] Still another object of the present invention is to provide a one-time feedback CMP process control method which is

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suitable for complex processes such as STI (shallow trench isolation) fabrication procedures.

[0020] Yet another object of the present invention is to provide an improved one-time feedback CMP process control method which eliminates or substantially reduces run-to-run process variations in a CMP process.

[0021] A still further object of the present invention is to provide an improved, one-time feedback CMP process control method which includes a one-time polishing time feedback adjustment for all wafers in a lot to facilitate greater between-wafer uniformity in the quantity of material removed from the wafers in a CMP process.

[0022] Yet another object of the present invention is to provide an improved CMP process control method which is characterized by precise adjustment in the process time and material removal rate in the chemical mechanical polishing of wafers.

[0023] A still further object of the present invention is to provide an improved CMP process control method which may include the polishing of pilot wafers in a lot to determine the divergence of the thickness of each wafer from a target thickness

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and the material removal rate of each polishing head in the apparatus; calculating a compensation time using the average divergence and the average material removal rate; calculating an update time by adding the compensation time to the original process time; and polishing the remaining wafers in the lot according to the update time.

[0024] Yet another object of the present invention is to provide an improved CMP process control method which in one embodiment includes determining a compensation time for each of multiple polishing heads or wafer carriers in a CMP apparatus using pilot wafers in a lot; calculating an update process time for each polishing head by adding the original process time to the compensation time for the polishing head; and processing remaining wafers in the lot using the update process time.

#### Summary of the Invention

[0025] In accordance with these and other objects and advantages, the present invention generally relates to an improved, one-time feedback CMP process control method which contributes to uniformity in the quantity of material removed from wafers in a lot during semiconductor processing and is suitable for complex processes such as STI (shallow trench isolation) fabrication procedures. According to one embodiment of the method, a pre-CMP

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thickness of each of multiple pilot wafers in a wafer lot is initially measured. The pilot wafers are then polished according to a default or given process recipe having a process time which is ordinarily used for the CMP process. After the CMP polishing sequence is completed, the post-CMP thickness of each pilot wafer is measured. Both the divergence of the post-CMP thickness of each wafer from a target thickness and the material removal rate of each polishing head in the apparatus are then determined.

[0026] According to an "average mode" of the CMP process control method, the average divergence between the post-CMP thicknesses and the target thicknesses of the pilot wafers, as well as the average material removal rate for the polishing heads, are determined. A compensation time is then calculated using the average divergence and the average material removal rate. An update time is calculated by adding the compensation time to the original process time. The remaining wafers in the lot are then polished according to the update time.

[0027] According to an "individual head mode" of the CMP process control method, the divergence between the target thickness and the post-CMP thickness produced by each of the multiple polishing heads in the CMP apparatus is determined. The material removal rate of each polishing head is also determined. Using the

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divergence and the material removal rate for each polishing head, a compensation time is calculated for each polishing head. An update time for each polishing head is calculated by adding the compensation time to the original process time for that polishing head. The remaining wafers in the lot are then processed using the calculated update time for each of the polishing heads.

[0028] Both the "average mode" and the "individual head mode" of the one-time feedback CMP process control method of the present invention can be carried out according to either a lot-based mode or a continuing mode. According to the lot-based mode, multiple pilot wafers in a lot are used to calculate the compensation time for the "average mode" or the "individual head mode", which is then implemented for the remaining wafers in the lot. Upon CMP processing of a new wafer lot, pilot wafers from that lot are then used to calculate a new compensation time only for the remaining wafers in the lot, and another compensation time is calculated for the wafers in the next lot.

[0029] According to the continuing mode, multiple pilot wafers in a lot are used to calculate the compensation time for the "average mode" or the "individual mode", which is implemented both for the remaining wafers in that lot and for some or all of the wafers in the next lot. A new compensation time is

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periodically calculated after numerous wafers in successive lots have been processed. The pilot wafers for the new compensation time may be selected from the beginning, middle or end of a lot.

#### Brief Description of the Drawings

[0030] The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

[0031] Figure 1 is a perspective view of a typical conventional chemical mechanical polishing apparatus for the simultaneous polishing of multiple wafers;

[0032] Figure 1A is a top perspective view, partially in section, of a conventional pedestal assembly of the CMP apparatus of Figure 1;

[0033] Figure 2 is a flow diagram illustrating a conventional, continuous process time feedback configuration for the CMP processing of multiple wafers;

[0034] Figure 3 is a flow diagram illustrating sequential process steps in the calculation of the post-CMP/target thickness divergence for each of multiple pilot wafers in a lot and the material removal rate for each of multiple polishing heads in a

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CMP apparatus, preparatory to operating the CMP apparatus in an "average mode" or an "individual head mode" according to the process of the present invention;

[0035] Figure 4 is a flow diagram illustrating sequential process steps in the operation of a CMP apparatus according to the "average mode" of the method of the present invention;

[0036] Figure 5 is a flow diagram illustrating sequential process steps in the operation of a CMP apparatus according to the "individual head" mode of the present invention;

[0037] Figure 6 is a schematic of a CMP apparatus, in implementation of the method of the present invention;

[0038] Figure 7 is a numerical depiction of successive wafers in two wafer lots, illustrating implementation of the method of the present invention according to a lot-based mode;

[0039] Figure 8 is a numerical depiction of successive wafers in multiple wafer lots, illustrating implementation of the method of the present invention according to a continuing mode;



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[0040] Figure 9 is a graph, wherein the post-CMP thickness of each of multiple wafers in a wafer lot, obtained using the conventional, continuous process time feedback configuration, is compared to the post-CMP thickness of each of the wafers obtained using the one-time feedback CMP process control method of the present invention;

[0041] Figure 10 is a cross-section of a dual-damascene structure suitable for implementation of the CMP process control method of the present invention; and

[0042] Figure 11 is a cross-section of an STI (shallow trench isolation) structure suitable for implementation of the CMP process control method of the present invention.

#### Detailed Description of the Invention

[0043] The present invention contemplates a one-time feedback CMP process control method which is used to polish each of successive wafers in one or more wafer lots, typically in the fabrication of semiconductor integrated circuits on the wafers. The method includes a one-time, rather than a continuous, feedback or update polish time adjustment to the polishing heads on the CMP apparatus for each of the successive wafers in the wafer lot. The update polish time adjustment is first obtained by processing

multiple pilot wafers and is then used to polish the remaining wafers in the lot or in successive lots. The method contributes to uniformity in the quantity of material removed from wafers in a wafer lot during chemical mechanical polishing of the wafers. The method is suitable for complex processes such as STI (shallow trench isolation) fabrication procedures, for example.

[0044] Referring to Figure 6, the one-time feedback CMP process control method of the present invention is carried out typically using a conventional CMP apparatus 10. The CMP apparatus 10 may include a base 12 on which is provided a first polishing platen 14a, a second polishing platen 14b and a third polishing platen 14c. A head rotation unit 18 is provided above the base 12. A first polishing head 20a, a second polishing head 20b, a third polishing head 20c and a fourth polishing head 20d are provided on the head rotation unit 18. A load cup 16 is provided on the base 12 for the loading of wafers onto and from the polishing heads 20a-20d. A PLC controller 22 is operably connected to the polishing platens 14a-14c and the polishing heads 20a-20d to control the polish time as well as polish pressure and other variables of each polishing step. It is understood that the method of the present invention may be equally adaptable to CMP apparatus of alternative design.

[0045] Referring next to Figures 3 and 6, according to the method of the present invention, the divergence between the post-CMP thickness and the target thickness of each of multiple pilot wafers 26 in a wafer lot 24 is initially determined. This is carried out by initially measuring the pre-CMP thickness of each of the pilot wafers 26, as indicated in step S1 of Figure 3, typically using a conventional metrology tool suitable for the purpose. Although four pilot wafers 26 are shown in the wafer lot 24 of Figure 6, it is understood that fewer or greater than four pilot wafers 26 may be used for the purpose. Preferably, at least two pilot wafers 26 are used.

[0046] The wafer lot 24 includes about 5~50 wafers. Typically, the wafer lot 24 includes about 25 wafers. Alternatively, the method of the present invention can be carried out using a batch of wafers, with each batch having typically about 40~500 wafers.

[0047] After the pre-CMP thickness of each pilot wafer 26 has been measured, the pilot wafers 26 are individually mounted on the respective polishing heads 20a-20d by operation of the load cup 16. As indicated in step S2 of Figure 3, using a standard or given (feedforward by pre-process) default polishing recipe, each of the pilot wafers 26 is then sequentially polished on the respective first polishing platen 20a, second polishing platen

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20b and third polishing platen 20c, as the head rotation unit 18 is re-positioned after each polishing step, in the direction indicated by the arrows 30. Accordingly, each pilot wafer 26 remains on the same polishing head 20a-20d throughout the polishing sequence. After completion of the polishing sequence, the post-CMP thickness of each pilot wafer 26 is measured, typically using conventional metrology techniques, as indicated in step S3.

[0048] As indicated in step S4, the divergence (D), or difference, between the target thickness and the post-CMP thickness of each pilot wafer is then determined. The material removal rate (R) of each polishing head 20a-20d on the CMP apparatus 10 is also determined (step S5). This is calculated by subtracting the post-CMP thickness from the pre-CMP thickness of each pilot wafer, and then dividing that value by the total polishing time. By use of the calculated values for the divergence (D) between the target thickness and the post-CMP thickness of each pilot wafer, and the material removal rate (R) of each polishing head 20a-20d, the CMP apparatus 10 can then be operated according to either the "average mode" or the "individual head mode", as hereinafter described.

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[0049] The CMP apparatus 10 is operated according to the "average mode" typically as shown in the flow chart of Figure 4. This is carried out by initially calculating the average divergence ( $D_{avg}$ ) of the pilot wafers from the target thickness of the wafers, as indicated in step S7, as well as the average material removal rate ( $R_{avg}$ ) of the polishing heads (step S8). A compensation time (Com-T) is then calculated (step 9), according to the following formula:

$$\text{Com-T} = (D_{avg}) / (R_{avg}) * k,$$

where Com-T is the compensation time,  $D_{avg}$  is the average divergence of the pilot wafers from the target thickness of the wafers,  $R_{avg}$  is the "average material removal rate of the polishing heads, and k is the compensation correction experimental factor which is correlated to layout, pattern density and integration process such as trench depth, sub-layer thickness ... etc.

[0050] As indicated in step S10, an update process time ( $T_U$ ) is then calculated by adding the compensation time to the original process time, according to the following formula:

$$T_U = T_o + \text{com-T},$$

where  $T_u$  is the update process time,  $T_o$  is the original process time and com-T is the compensation time calculated at step S9.

[0051] As indicated in step S11, the remaining wafers 28 in the wafer lot 24 are then polished using the update process time ( $T_o$ ) calculated at step S10, by operation of the CLC controller 22.

[0052] The CMP apparatus 10 is operated in the "individual head mode" typically as shown in the flow chart of Figure 5. The "individual head mode" is an alternative to the "average mode" outlined above with respect to Figure 4. As indicated in step S7a, the compensation time ( $Com-T_i$ ) for each polishing head 20a-20d is initially calculated according to the following formula:

$$Com-T_i = (D_{avg_i}) / (R_{avg_i}) * k_i,$$

where  $D_{avg_i}$  is the average divergence between the post-CMP thickness and the target thickness of the plural wafers polished using each polishing head (calculated according to step S4 in Figure 3),  $R_i$  is the material removal rate of each polishing head (calculated according to step S5 in Figure 3), and  $k_i$  is the compensation correction experimental factor of each polish carrier which is correlated to layout, pattern density, head construction and integration process such as trench depth, sub-layer thickness ... etc.

[0053] As indicated in step S7b, an update process time for each polishing head is then calculated by adding the compensation time to the original process time, according to the following formula:

$$T_{Ui} = T_{oi} + com - T_i,$$

where  $T_{Ui}$  is the update process time for each polishing head,  $T_{oi}$  is the original process time for each polishing head and  $com - T$  is the compensation time for each polishing head, calculated at step 7a. As indicated in step S7c, the remaining wafers 28 in the wafer lot 24 are then processed using the update process time ( $T_{Ui}$ ) calculated for each corresponding polishing head 20a-20d in the CMP apparatus 10. Accordingly, the CLC controller 22 controls each polishing head 20a-20d according to the update process time calculated for that polishing head, throughout the polishing sequence for the remaining wafers 28.

[0054] In a preferred embodiment, the CLC controller 22 is provided with supporting software to implement steps S1-S6 of Figure 3, as well as a selector option between the "average mode" of Figure 4 and the "individual head mode" of Figure 5 and the capability to carry out the sequential process steps of each, according to the knowledge of those skilled in the art.

[0055] Referring next to Figure 7, the CMP apparatus 10 can be operated according to a lot-based mode using either the "average

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mode" of Figure 4 or the "individual head mode" of Figure 5. According to the lot-based mode, the multiple pilot wafers 26 in the wafer lot 24 are used to calculate the compensation time for the "average mode", as detailed herein above with respect to Figure 4, or the "individual head mode", as detailed herein above with respect to Figure 5. The compensation time is then implemented for the remaining wafers 28 in the wafer lot 24. Upon CMP processing of a new wafer lot 24, pilot wafers 26 from that lot 24 are then used to calculate a new compensation time only for the remaining wafers 28 in the lot 24, and another compensation time is calculated for the wafers 24 in the next lot 24.

[0056] Referring next to Figure 8, the CMP apparatus 10 can be operated according to a continuation mode. Multiple pilot wafers 26 in a wafer lot 24 are used to calculate the compensation time for the "average mode" or the "individual mode", which is implemented both for the remaining wafers 28 in that lot and for some or all of the wafers in the succeeding lot. A new compensation time is periodically calculated after numerous wafers in successive lots have been processed. The pilot wafers for the new compensation time may be selected from the beginning, middle or end of a lot.



[0057] Referring next to Figure 9, a graph is shown wherein post-CMP thickness of each of multiple wafers in a lot, as a result of two separate CMP processes, is plotted against the individual successive wafers, by number, in the lot. A CMP process in which was implemented the conventional, continuous feedback mechanism, heretofore described with respect to Figure 2, is shown Fig 901. A CMP process in which was implemented the single-feedback CMP process control method of the present invention is shown Fig 9-2.

[0058] The target thickness of each of the CMP processes, the results of which are shown in Figure 9, was 840 angstroms. It can be seen from the graph that the one-time feedback mechanism of the present invention results in a post-CMP thickness which much more closely approximates the target thickness, as compared to the conventional continuous feedback mechanism.

[0059] Referring next to Figure 10, the CMP process control method of the present invention is suitable for the chemical mechanical planarization of a metal layer 48 in a dual-damascene structure 34. The dual damascene structure 34 typically includes a first cap layer 39 deposited on a conducting layer 36, then followed by first dielectric layer 38 deposited above it. An etch stop layer 40 deposited on the first dielectric layer 38, and a second dielectric layer 42 deposited on the etch stop layer

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40 can also be included in the structure. Each of one or more trenches 50 is lined with a barrier layer 44, and a seed layer 46 lines the barrier layer 44. The metal layer 48 fills the trench or trenches 50.

[0060] The metal layer 48 is typically tungsten, copper or aluminum, or an alloy of these metals. Each trench 50 has a depth of from typically about 1000 angstroms to about 3  $\mu\text{m}$ . The first dielectric layer 38 and the second dielectric layer 42 each is typically a low dielectric material such as FSG, BD, silk or HSQ. The barrier layer 44 may be any suitable metal or material such as Ta, TaN or TiN. The cap layer 40 may be any suitable material such as SiN, SiC or N free ARC.

[0061] Referring next to Figure 11, the CMP process control method of the present invention is suitable for planarizing an oxide layer 56 on an STI (shallow trench isolation) structure 54. The STI structure 54 includes a p+ type silicon substrate or epi. A trench oxide 68, lined by a liner oxide 66, separates an n-well 62 from a p-well 64. The oxide layer 56 has a thickness of typically about 2,000~15,000 angstroms. Each trench oxide 68 has a depth of typically about 1,000~10,000 angstroms.

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[0062] While the preferred embodiments of the invention have been described above, it will be recognized and understood that various modifications can be made in the invention and the appended claims are intended to cover all such modifications which may fall within the spirit and scope of the invention.